The Human Brain Project (HBP) is a European Commission Future and Emerging Technologies Flagship that aims to achieve a multi-level, integrated understanding of brain structure and function through the development and use of information and communication technologies (ICT). These technologies will enable large-scale collaboration and data sharing, reconstruction of the brain at different biological scales, federated analysis of clinical data to map diseases of the brain, and the development of brain-inspired computing systems.
The HBP is working to achieve an integrated, multi-level understanding of brain structure and function through the development and use of information and communication technologies (ICT).

The HBP’s ICT Platforms will allow neuroscientists, clinical researchers and information technology developers to perform diverse experiments and share knowledge, with a common goal of unlocking the most complex structure in the known universe. During the first two-and-a-half years (the Ramp-Up Phase), the HBP will collect strategic data, develop theoretical frameworks and perform the development work necessary to make the six ICT Platforms available for use by the scientific community in the Operational Phase. The HBP’s ICT Platforms are:

- **Neuroinformatics (a data repository, including brain atlases)**
- **Brain Simulation (building ICT models and simulations of brains and brain components)**
- **Medical Informatics (bringing together information on brain diseases)**
- **Neuromorphic Computing (ICT that mimics the functioning of the brain)**
- **Neurorobotics (testing brain models and simulations in virtual environments)**
- **High Performance Computing (this platform will support the other Platforms)**

The HBP was launched in 2013 and brings together more than 100 academic and corporate Partners in more than 20 countries. HBP research is organised into twelve Subprojects (SP), each broken down into Work Packages (WP) and Tasks (T), with well-defined goals and milestones. Six Subprojects are building the ICT Platforms, while the other six are gathering data, clarifying theory and controlling ethical aspects. An additional Subproject manages and coordinates the HBP.

With an unprecedented cross-disciplinary scope, the HBP’s goal is to catalyse a global collaborative effort to understand the human brain and its diseases and, ultimately, to emulate its computational capabilities.

The HBP is designing and implementing a Neuromorphic Computing Platform to allow non-expert neuroscientists and engineers to perform experiments with configurable Neuromorphic Computing Systems (NCS). These NCS implement simplified versions of brain models developed on the Brain Simulation Platform (SP6) as well as on generic circuit models. The NCS are hardware devices incorporating state-of-the-art electronic component and circuit technologies, as well as new knowledge arising from other areas of HBP research (experimental neuroscience, theory, brain modelling). The Platform will provide NCS based on physical (analogue or mixed-signal) emulations of brain models (NM-PM), running in accelerated mode, numerical models running in real time on digital multicore architectures, (NM-MC), and the software tools necessary to design, configure and measure the performance of these systems. The Platform will be tightly integrated with the High Performance Computing Platform (SP7), which will provide essential services for mapping and routing circuits to neuromorphic substrates, benchmarking and simulation-based verification of hardware specifications.

The primary objective of this Subproject for the Ramp-Up Phase is to construct a first fully operational version of the HBP Neuromorphic Computing Platform. The Platform will consist of two complementary, large-scale NCS built in custom hardware at locations in Heidelberg, Germany (the NM-PM system) and Manchester, United Kingdom (the NM-MC system). The Platform will provide remote access to both NCS, software tools for their configuration, operation and the analysis of generated data as well as user support documentation, training workshops and a consulting service. Platform users will be able to study network implementations of their choice including simplified versions of brain models developed on the Brain Simulation Platform or generic circuit models based on theoretical work. As a secondary objective the Subproject will develop the technologies required to build the next generations of the Platforms planned for the Operational Phase of the HBP after successful completion of the Ramp-Up Phase.

**Operational Objectives**
In the Ramp-Up Phase, SP9 is constructing two operational NCS. This work is methodologically based on two previous successful and internationally recognised research projects. The two systems are operating using the framework of the Neuromorphic Computing Platform, which provides software tools and user support. Finally, SP9 is exploring some of the technologies needed for future upgrades of the NCS. The work required to build and manage the Platform can be summarised as follows:

The HBP Physical Model Neuromorphic System Version 1 (NM-PM-1) in Heidelberg (Germany). The HBP Physical Model Neuromorphic System Version 1 (NM-PM-1) in Heidelberg (Germany). The NM-PM-1 system is based on the European FACETS project, which pioneered an approach combining local analogue computation in neurons and synapses with binary, asynchronous, continuous time spike communication. Current systems incorporate $50^{10^6}$ plastic synapses and 200,000 biologically realistic neurons models on a single 6-inch silicon wafer in 180nm process technology. The system does not execute programmed code but evolves according to the physical properties of the electronic devices. FACETS has also pioneered a network description language (PyNN) that provides Platform independent access to software simulators and neuromorphic systems and will be used throughout the HBP. BrainScaleS – a follow-up project – is pioneering the use of the technology to replicate behaviour and learning over periods of up to a year while simultaneously emulating the millisecond-scale dynamics of the system. During the Ramp-Up Phase, the system is being scaled up to a size of 20 wafers corresponding to 4 million neurons and 1 billion synapses operating 10,000 times faster than biological real time. This system is called NM-PM-1 and will be under construction until Month 18 of the Ramp-Up Phase. It will be installed in a dedicated building on the Im Neuenheimer Feld Science Campus at Heidelberg University in Germany. The NM-PM-1 system will be complemented by a dedicated computational cluster for network configuration, data analysis and execution of closed perception-action loop experiments.

The HBP Multi-Core Neuromorphic System Version 1 (NM-MC-1) in Manchester (United Kingdom). The HBP’s NM-MC-1 system is based on the approach adopted by the UK SpiNNaker group. The group has a strong grounding in the ARM architecture – which offers an excellent basis for scalable digital many-core systems operating at real time with low power – has recently completed the integration of a SpiNNaker chip into an operational system and is now running experiments. Each chip has 18 cores and a shared local 128MB RAM, and allows real-time simulation of networks implementing complex, non-linear neuron models. A single chip can simulate 16,000 neurons with eight million plastic synapses running in real time with an energy budget of 1W. During the Ramp-Up Phase, SP9 will be scaled up to a size of 1 million ARM CPU cores corresponding to approximately 56,000 SpiNNaker chips with a simulated bisection bandwidth of 10 billion spikes per second. The system can simulate 1 billion neurons in biological real time. This system is called NM-MC-1 and will be available in Month 18 of the Ramp-Up Phase.

The Neuromorphic Computing Platform. The Neuromorphic Computing Platform is the HBP infrastructure that will provide remote access and user support for the two NCS described above. To achieve this goal, SP9 is developing two major lines of activity: the first is dedicated to the development of software tools, and the second focuses on the implementation of an user access concept. All users will be expected to describe their circuits in the PyNN description language, which is being further developed to match the needs of the two NCS. NM-PM-1 will also need specific software for mapping, routing, calibration, database access and closed loop experiments. SP9 is developing this software. After finalisation of the construction phase for the two systems in Month 18, SP9 will provide web-based access, documentation and training for users.

Novel technologies for neuromorphic circuits. Although most of SP9’s effort during the Ramp-Up Phase is directed at building and operating the Platform and the two NCS, the Subproject is also developing technologies for phases 2 and 3. This includes the development of a lamination technology to integrate silicon wafers into a layer structure of printed-circuit boards, the development of CAE tools for the design of massively parallel VLSI systems, and the evaluation of neuromorphic technologies developed outside the HBP.
The two Neuromorphic Computing Systems being constructed during the Ramp-Up Phase in Heidelberg (NM-PM-1) and Manchester (NM-MC-1) constitute key computing resources for the HBP. A conventional local compute cluster in Heidelberg complements the NM-PM-1 system. The cluster is located in the NM-PM-1 building and features 128 Intel i7-2600 cores with a total Linpack benchmark performance of 3.2 Teraflops for computation. The cluster is being optimised for efficient communication with the NM-PM-1 wafer system and includes 52 i7-nodes dedicated to operating the high-speed links to individual wafers for closed-loop virtual robotics experiments. Close physical proximity to the NM-PM-1 is a prerequisite for the required low latency communication. Users will access the Platform via a single point of access (a web portal) shared among all the Platforms.

Computer Resources

HBP Neuromorphic Computing System NM-PM-1

- 20 Neuromorphic Wafers
- 0.02 Exa-connections/s
- 4 Million Neurons
- 1 Billion Synapses
- Acceleration x 10.000

HBP NM-PM-1 Conventional Compute Cluster

- 160 Intel Haswell Cores
- 4 TeraFlop/s
- 1 Tbit/s

Computer resources for the Neuromorphic Computing Platform (PM)

103 machine: 864 cores, 1 PCB, 75W
104 machine: 10,368 cores, 1 rack, 900W
105 m/c: 103,680 cores, 1 cabinet, 9kW

(NB 12 PCBs for operation without aircon)
Deliverables

MONTH 6 – REPORT
NEUROMORPHIC COMPUTING
PLATFORM V1 – SPECIFICATION DOCUMENT

This report provides a detailed specification of the Neuromorphic Computing Platform v1, the two NCS (NM-PM and NM-MC) and the software tools incorporated in the Platform. An annex provides a description of work preparing for later versions of the Platform. The report specifies indicators of progress and target values for the indicators.

MONTH 12 – REPORT
NEUROMORPHIC COMPUTING
PLATFORM V1 – SET-UP DOCUMENT

This report describes progress in the development of the Platform, and related software tools.

MONTH 18 – PROTOTYPE
NEUROMORPHIC COMPUTING PLATFORM V1 – PRELIMINARY RELEASE FOR INTERNAL CONSORTIUM USE

This will be the first release of the Platform, and will be available for use by members of the HBP Consortium. The release will incorporate both neuromorphic computing systems (NM-PM and NM-MC) and the software tools required to configure neuromorphic systems, to simulate their operation and to test their performance.

MONTH 30 – PROTOTYPE
NEUROMORPHIC COMPUTING PLATFORM V1

This will be the first release of the Platform, for use by scientists outside the HBP Consortium. The release will incorporate both neuromorphic computing systems (NM-PM and NM-MC) and the software tools required to configure neuromorphic systems, to simulate their operation and to test their performance.

MONTH 30 – REPORT
NEUROMORPHIC COMPUTING PLATFORM V1 – DOCUMENTATION

The prototype will be accompanied by technical and user documentation facilitating use of the Platform by users within and outside the HBP Consortium and by a roadmap describing plans for future development in the Operational Phase of the Project.
Physical and Many Core Neuromorphic Computing Systems ready for serial production; Neuromorphic Computing Platform fully specified

Software tools for Neurmorphic Computing Systems demonstrated


Remote user access to NM-PM-1 and NM-MC-1 available


MONTH 6
- NM-PM-1 ready for serial production; NM-MC-1 ready for serial production
- Software tools for neuromorphic computing fully specified; Detailed specification of research activities on novel neuromorphic technologies
- Neuromorphic Computing Platform fully specified
- Requirements for user documentation and support for the Neuromorphic Computing Platform, guidelines for establishing alliances

MONTH 12
- Software tools for NM-PM and NM-MC demonstrated
- Identification of potential alliances on neuromorphic computing

MONTH 18
- NM-PM-1 construction completed, start of commissioning

MONTH 24
- NM-MC-1 construction completed, start of commissioning
- Neuromorphic Computing Platform ready for internal release
- Guidebook for the use of the Neuromorphic Computing Platform (internal release)

MONTH 30
- Software tools for Neuromorphic Computing Systems demonstrated
- Public platform launched, software model for NM-MC-2 specifications
- Review of novel technology developments
- Neuromorphic Computing Platform ready for community release
- Guidebook for the use of the Neuromorphic Computing Platform
Work Packages and Key Personnel

WP9.1: Neuromorphic Computing with Physical Emulation of Brain Models

- Development and implementation of VLSI circuits emulating neurons and synapses
  Karlheinz MEIER - UHEI
- Development and implementation of high density configurable VLSI spike communication networks
  Karlheinz MEIER - UHEI
  Rene SCHÜFFNY - TUD
- Development and implementation of neuromorphic systems-on-chip - SOCs
  Karlheinz MEIER - UHEI
  Yusuf LEBLEBICI - EPFL
  Volkan OZGUZ - SU
  Yasar GÜRBÜZ - SU
- Integration of the neuromorphic SOCs into the NCS framework
  Karlheinz MEIER - UHEI
  Rene SCHÜFFNY - TUD
  Ulrich BRÜNING - UHEI
- Development of low level software and firmware for the neuromorphic system
  Karlheinz MEIER - UHEI
  Rene SCHÜFFNY - TUD

WP9.2: Neuromorphic Computing with Digital Many-core Implementation of Brain Models

- Design and implementation of digital many-core processor systems for neuromorphic computation
  Steve FURBER - UMAN
  Sebastian HÖPPNER - TUD
  Yusuf LEBLEBICI - EPFL
  Volkan OZGUZ - SU
  Yasar GÜRBÜZ - SU
- Design and implementation of digital networks for communication between neurons
  Steve FURBER - UMAN
  Sebastian HÖPPNER - TUD
  Yusuf LEBLEBICI - EPFL
- Integration
  Steve FURBER - UMAN
  Yusuf LEBLEBICI - EPFL
  Sebastian HÖPPNER - TUD
  Volkan OZGUZ - SU

Subproject Co-Leaders

Karlheinz MEIER, Steve FURBER
**Programming models for digital many-core neuromorphic systems**

Steve FURBER - UMAN  
Enrico MACII - POLITO

**Software Tools for Neuromorphic Computing**

Andrew DAVISON - CNRS

**NCS integration with the HBP databases, the HBP simulation cockpit, HBP analysis tools and the HBP Neurorobotics Platform**

Andrew DAVISON - CNRS  
Steve FURBER - UMAN  
Karlheinz MEIER - UHEI

**Simplifying brain models**

Karlheinz MEIER - UHEI  
Andrew DAVISON - CNRS

**Mapping and routing of imported circuits to the NCS**

Karlheinz MEIER - UHEI  
Steve FURBER - UMAN  
Erwin LAURE - KTH  
Rene SCHÜFFNY - TUD  
Andrew DAVISON - CNRS

**Benchmarking the neuromorphic circuits developed in WP9.1 and WP9.2**

Karlheinz MEIER - UHEI  
Steve FURBER - UMAN  
Anders LANSNER - KTH  
Andrew DAVISON - CNRS

**Executable system specification for the neuromorphic circuits developed in WP9.1 and WP9.2**

Karlheinz MEIER - UHEI  
Andrew DAVISON - CNRS  
David LESTER - UMAN  
Rene SCHÜFFNY - TUD

**Novel Technologies for Neuromorphic Circuits**

Yusuf LEIBLEBICI - EPFL

**High-density connection technologies for the integration of silicon substrates with PCB technologies**

Oswin EHRMANN - FG

**Neuromorphic Computing Platform: integration and operations**

Karlheinz MEIER - UHEI  
Steve FURBER - UMAN

**Development of the specification for the Neuromorphic Computing System**

Karlheinz MEIER - UHEI

**Neuromorphic Computing Systems – component acquisition, production and manufacturing**

Karlheinz MEIER - UHEI  
Volkan OZGUZ - SU

**Neuromorphic Computing Systems – assembly, operation & maintenance**

Karlheinz MEIER - UHEI

**Software for Neuromorphic Computing Systems and for configuring Neuromorphic Computing Systems**

Karlheinz MEIER - UHEI  
Anders LANSNER - KTH  
Andrew DAVISON - CNRS  
Steve FURBER - UMAN

**NM Platform website construction and maintenance**

Karlheinz MEIER - UHEI

**Neuromorphic Computing Platform: user support and community building**

Karlheinz MEIER - UHEI

**Neuromorphic Computing service centre for user training and user support; documentation**

Karlheinz MEIER - UHEI  
Steve FURBER - UMAN

**Scientific coordination and support**

Karlheinz MEIER - UHEI

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**SP9 Objective**

“A Neuromorphic Computing Platform that allows non-expert neuroscientists and engineers to perform experiments with configurable Neuromorphic Computing Systems (NCS) implementing simplified versions of brain models.”

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**WP9.5**

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<tr>
<th>Activity</th>
<th>Principal Investigator</th>
<th>Co-Investigators</th>
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<tr>
<td>Development of the specification for the Neuromorphic Computing System</td>
<td>Karlheinz MEIER - UHEI</td>
<td>Steve FURBER - UMAN</td>
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<tr>
<td>Neuromorphic Computing Systems – component acquisition, production and manufacturing</td>
<td>Karlheinz MEIER - UHEI</td>
<td>Volkan OZGUZ - SU</td>
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<tr>
<td>Neuromorphic Computing Systems – assembly, operation &amp; maintenance</td>
<td>Karlheinz MEIER - UHEI</td>
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</table>
| Software for Neuromorphic Computing Systems and for configuring Neuromorphic Computing Systems | Karlheinz MEIER - UHEI  
Anders LANSNER - KTH  
Andrew DAVISON - CNRS  
Steve FURBER - UMAN |
| NM Platform website construction and maintenance | Karlheinz MEIER - UHEI |

**WP9.6**

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<tr>
<td>Neuromorphic Computing Platform: user support and community building</td>
<td>Karlheinz MEIER - UHEI</td>
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</table>
| Neuromorphic Computing service centre for user training and user support; documentation | Karlheinz MEIER - UHEI  
Steve FURBER - UMAN |

**WP9.7**

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<th>Principal Investigator</th>
<th>Co-Investigators</th>
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<tr>
<td>Scientific coordination and support</td>
<td>Karlheinz MEIER - UHEI</td>
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</table>
Steve Furber leads the Advanced Processor Technologies group at the University of Manchester and is known internationally for having spearheaded the creation of the ARM microprocessor at Acorn Computer, Ltd. His current research focuses on energy-efficient processor and System-on-Chip technology, including the EPSRC SpiNNaker (Biologically-Inspired Massively-Parallel Architectures - BIMPA) project, which he directs. This multi-site initiative, developed in collaboration with the Universities of Southampton, Cambridge and Sheffield, uses large arrays of bespoke energy-optimised many-core processors to model large-scale brain functions in real time. Prof. Furber has been elected to an IEEE Fellowship and is a member of the Academia Europaea. He chairs the REF 2014 sub-panel B11 and the Royal Society study of computing in schools. Prof. Furber co-directs the HBP Neuromorphic Computing Subproject.

Karlheinz Meier is the founding director of the Kirchhoff-Institute for Physics and the ASIC Laboratory for Microelectronics, where he holds a chair in experimental physics. With a strong background in instrumentation for particle physics and neuro-inspired computation he has 28 years of post-doctoral experience in large-scale experimental research. Coordinator of the FACETS, FACETS-ITN and BrainScaleS projects, he has been project leader for the PreProcessor data processing system for the ATLAS experiment at the LHC in CERN (Switzerland) and a leading contributor to four major particle physics experiments at the DESY (Germany) and CERN laboratories. He has supervised more than 30 Ph.D. theses and published more than 400 research papers (H-index of 64). He is a board member of the German Physical Society and member of the Samsung Advanced Institute of Technology. Prof. Meier co-directs the HBP Neuromorphic Computing Subproject.
Ulrich Brüning is a professor of computer architecture at the University of Heidelberg, Computer Architecture Group (CAG). He studied electrical engineering at the Technische Universität Berlin, where he led the hardware development of innovative computer architectures. His research interests include Interconnection Networks ASIC Design.

Andrew P. Davison is a senior research scientist (CR1) in the Unité de Neurosciences, Information and Complexité (UNIC) of the Centre National de la Recherche Scientifique, France, CNRS where he leads the Neuroinformatics group. His research interests focus on biologically detailed modelling, simulating neuronal networks (particularly the mammalian visual system), and developing tools to improve the reliability, reproducibility, and efficiency of biologically realistic simulation. Davison has a PhD in computational neuroscience from the University of Cambridge.

Oswin Ehrmann is the head of the Department of High Density Interconnect and Wafer Level Packaging (HDI&WLP) at the Fraunhofer IZM in Berlin. He obtained a degree in physics from the Technical University of Berlin, has 25 years of experience in packaging technologies and has managed several national and international projects.

Yasar Gürbüz received a B.S. degree in electrical engineering from Erciyes University in 1990, an M.S. degree in 1993 and Ph.D. degree in 1997 in electrical engineering from Vanderbilt University in the USA. He worked as a senior research associate at Vanderbilt between 1997 and 1999. From 1999 to 2000, he worked at Aselsan Inc. He joined Sabanci University as a faculty member in the Faculty of Engineering and Natural Sciences in 2000. His research focuses on microelectronic systems and includes RF/microwave integrated circuits/systems, analogue- and mixed-signal integrated circuits, microelectromechanical systems (MEMS), and solid-state sensors and actuators. He is a member of IEEE and SPIE.
Sebastian Höppner received the Dipl.-Ing. (M.Sc.) in Electrical Engineering from Technische Universität Dresden, Germany in 2008. He is currently working as technical manager with the Chair of Highly-Parallel VLSI-Systems and Neuromorphic Circuits at TU Dresden. His research interests include circuit design for clocking, data transmission and power management in low power systems-on-chip and design methodology for analogue CMOS circuits. He has five years of experience in designing full-custom circuits for multi-processor systems-on-chip (MPSoCs), like ADPLL clock generators, register files and high-speed on-chip links, in academic and industrial research projects. He was the manager of the full-custom circuit design group for six MPSoC chips in 65nm and 28nm CMOS technology. He is the author or co-author of more than 20 publications and five patents (two issued, three pending) in the above fields.

Anders Lansner is the Chair of Computer Science at KTH, and the founding director of its Department of Computational Biology, where he specialises in computational neuroscience and neurocomputing. With 25 years of post-doctoral experience in creating and carrying out field research, Prof. Lansner has forged extensive collaborations with experimental neuroscientists and psychologists, nationally and internationally. He is a Member of the Royal Swedish Academy of Engineering Sciences (IVA) and Swedish board member of INCF (International Neuroinformatics Coordinating Facility). He has supervised more than 20 Ph.D. theses and numerous Masters theses.

Erwin Laure leads the PDC Center for High Performance Computing at KTH, and is also the co-director of the OGF Data Area, a former co-chair and co-founder of the OGF GIN-Community Group and a member of the external advisory board of the D4Science-II. He holds a Ph.D in Business Administration and Computer Science from the University of Vienna (Austria) and before joining PDC was Technical Director of the EU funded projects “Enabling Grids for E-Science in Europe” II and III (EGEE-II and-III) at CERN. Along with heading the PDC, his research interests include Grid computing, programming environments, languages, compilers and runtime systems for parallel and distributed computing.

Yusuf Leblebici has degrees from Istanbul Technical University and the University of Illinois at Urbana-Champaign (UIUC) and has been active in the field of computer and electrical engineering since 1990. Between 1991 and 2001, he worked as a faculty member at UIUC, at Istanbul Technical University, and at Worcester Polytechnic Institute (WPI). Since 2002, he has been a Chair Professor at EPFL, and director of the Microelectronic Systems Laboratory. His research interests include the design of high-speed CMOS, digital and mixed-signal integrated circuits, computer-aided design of VLSI systems, intelligent sensor interfaces, modelling and simulation of semiconductor devices, and VLSI reliability analysis. He has authored five major textbooks on VLSI circuits, and received many honours from the IEEE.
David Lester earned a BA in mathematics and a DPhil at the Programming Research Group in Oxford, and began his working life as the Project Leader of ESPRIT-415B programming a distributed implementation of Functional Languages using Transputers with GEC-Marconi. In 1990 he joined Manchester University as a Lecturer specialising in Functional Programming, Computer Arithmetic, and more recently Neuromorphic Engineering. His role in the Human Brain Project is to direct the software aspects required to make NM-MC1 and NM-MC2 platforms usable.

Enrico Macii holds a Dr. Eng. degree in Electrical Engineering, a Dr. Sc. degree in Computer Science and a Ph.D. degree in Computer Engineering from the University and Politecnico di Torino. His research interests are focussed on the design of digital circuits and systems, with particular emphasis on low-power design. He has authored over 350 scientific publications including the book: “Ultra Low-Power Electronics and Design,” and has received awards for his publications at various IEEE forums. He has been on the editorial board of various reputed journals, has chaired a large number of programmes and symposia, and has set up collaborations with several large companies, including FIAT, Hewlett-Packard and Intel. His major research contributions include: design solutions and methods for leakage and dynamic power optimisation; design techniques and methods for thermal control; and design solutions for limiting NBTI and aging effects in nanometre CMOS circuits and systems. Recently, he has extended the scope of his research to include bioinformatics.

Volkan Ozguz is the Director of the Nanotechnology Research and Application Center at Sabanci University. A former Chief Technology Officer and Senior Vice President at Irvine Sensors Corporation, he has been working in the semiconductor technology, packaging, microelectronics manufacturing and nanotechnology fields since 1979. He received his BS and MSc degrees from Istanbul Technical University, his Ph.D. in electrical engineering from North Carolina State University (USA), and has been a Fulbright and NATO Fellow. His experience in the design and implementation of microelectronic, nanoelectronic and neuromorphic systems spans fabrication technologies, process design and integration, facility operations and technology transfer. Dr. Ozguz has authored more than 70 journal articles, conference publications and book chapters. He has 16 patents and many patent applications.

Johannes Schemmel is a senior post-doctoral researcher at the Kirchhoff Institute for Physics. He has 15 years of post-doctoral experience in designing neuromorphic microelectronics systems for brain-inspired information processing. He pioneered the FACETS and BrainScaleS chip and systems architectures. Dr. Schemmel is the leader of HBP WP9.1, which is focused on designing and constructing the physical model system of the HBP Neuromorphic Platform.
Rene Schüffny received a Dr.-Ing (Ph.D.) and a Dr.-Ing. habil. (D.Sc.) degree from the Technische Universität Dresden (Germany). Since 1997, he has held the Chair of Highly-Parallel VLSI-Systems and Neuromorphic Circuits at TUD. He is the author or co-author of numerous publications, and has acted as a reviewer for several international journals.
SP9 is designing a new category of computing hardware inspired by the circuitry of the brain to overcome the fundamental limits of conventional technology. Like the brain, the new hardware will consist of many computing units operating in parallel. Integrating the hardware with software, the Neuromorphic Computing Platform will make intensive use of high-performance computing services from SP7 and provide access to two complementary kinds of system. The first will be built from very fast, energy-efficient analogue devices that emulate the physical processes going on in the brain; the second will be based on very large numbers of digital computing devices. The two systems will be highly configurable, making it possible to simulate different models of the brain without re-engineering the hardware. The same hardware will make it possible to simulate simplified versions of the detailed brain models produced in SP6 as well as more abstract models developed in SP4. The new hardware, which will complement current computing technology, has the potential to enable completely new applications in industry, services, transport, and healthcare. The Neuromorphic Computing Platform will provide the capabilities developers need to explore these applications.